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EXAMINER	
FLORES, LEON	

ART UNIT	PAPER NUMBER
2611	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/758,863	STASZEWSKI ET AL.	
	Examiner	Art Unit	
	LEON FLORES	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 January 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-54* is/are pending in the application.

4a) Of the above claim(s) *4* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-54* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims (1-47) have been considered but are moot in view of the new ground(s) of rejection.

Response to Remarks

Applicant asserts that, *"the EARLY/LATE phase detector output signal in Girardeau does not satisfy Claim 1 's limitation "wherein the signal has a high degree of correlation with an RF output of the RF circuit". "Signal ... correlation with all RF output", as required by Claim 1, necessitates that the phase detector output correlates with the frequency drift of the oscillator. Such is not the case with Girardeau's oscillator 23. Girardeau's phase detector output is a sign of the phase relationship between the reference oscillation 26 and the feedback oscillation 28 synchronous to the reference oscillation 26 clock. That 1-bit (only early/late information) signal cannot possibly correlate with the frequency deviation of the output of oscillator 23. Reason one; 1-bit of information cannot have a "high degree of correlation" with the frequency drift. Reason two, the 1-bit signal is a sign of phase, which is time integral of frequency, and even the full resolution of the phase error can not be correlated to the frequency drift, without first integrating it. Accordingly, resolution of the phase error and integrating the phase error are not taught in Girardeau since there would be no motivation of doing so".*

The examiner respectfully agrees. However, a new ground of rejection has been issued in order to substantiate for this limitation.

Applicant further asserts that, *"Yamaguchi shows in Figure 29 a spectrum analyzer connected to the output of a "phase detector." This example, however, is irrelevant to the claimed invention for the following reasons: 1. Yamaguchi teaches measuring jitter of an external clock connected to Phase Detector that forms a PLL loop together with Signal Generator to generate the other Phase Detector input ("A clock signal under test is inputted to a phase detector as a reference frequency." col. 15, lines 30-32; and "In this case, the phase detector and the signal generator compose a phase-locked loop." col. 15, lines 32-33). This teaching in Yamaguchi clearly states that the phase detector itself would be useless since the other phase detector input (non-"reference" or variable) needs to be created as well as a means to perform phase locking to the "reference" input. 2. The above requirement to form a PLL loop with the Phase Detector stems from the fact that Yamaguchi teaches measuring jitter of an external clock. In contrast, the present invention does not concern itself with measuring performance of some external, unrelated clock. Rather, it deals with measuring performance of a signal generated by the RF circuit by observing and manipulating signals from within the RF circuit. In the embodiment examples in Figures 2 (frequency synthesizer) and 3 (frequency synthesizer-based transmitter) of the instant application, the PLL is part of the RF circuit itself. The performance of these RF circuits does not simply depend on one clock - it is a combination of the reference clock, variable clock generated by the DCO within the RF circuit, as well as the PLL loop parameter settings. 3. "An RMS jitter JRMS of a clock signal is measured in frequency domain." (col. 15, lines 27-28). In contrast, the present invention operates in the time domain and does not*

need to resort to operating in the frequency domain"

The examiner respectfully disagrees. The concept of measuring and observing the phase detector output outside of a PLL is taught by the reference of Yamaguchi. (See fig. 29) One skilled in the art would have founded obvious to connect a spectrum analyzer to a PLL in order to measure and observe the output of the phase detector, as taught by Yamaguchi. This PLL could have been located in a transmitter or receiver.

Applicant further asserts that, *"Girardeau shows in Figure 1 a digital phase locked loop (DPLL), which comprises a phase detector 12 that produces two 1-bit digital signals EARLY 30 and LATE 32, which the Examiner improperly equates to the phase error. These signals are a very crude representation of the phase relationship between the reference oscillation 26 and feedback oscillation 28 and only indicate which phase detector input is ahead of the other with no information of how much (col. 2, lines 50-61). Thus, only the sign of the phase error is produced with the actual magnitude or value missing. The EARLY and LATE signals cannot be equated with the phase error of the instant application, which has information of the actual phase error value".*

The examiner respectfully disagrees. In col. 2, lines 50-61 the reference does teach that comparator 12 produces an early error signal when the feedback leads the reference. However, when the reference leads the feedback comparator 12 produces a late error signal. Furthermore, fig. 1 element 12 does teach a comparator or phase detector.

Applicant further asserts that, *"there is no correlation in Girardeau between the 1-bit phase detector 12 output 30/32 with the frequency drift of the oscillator 23, the*

discussion of the transfer function flatness is irrelevant. If, arguendo, the phase detector would produce full resolution phase error and the system somehow made to work, then, the transfer function would not be fiat as a result of the frequency being the time derivative of phase".

The examiner respectfully agrees. However, a new ground of rejection has been issued in order to substantiate for this limitation.

Applicant further asserts that, *"Claim 41 requires and positively recites, a circuit comprising: "a reference phase accumulator coupled to a signal input, the reference phase accumulator containing circuitry to compute a reference phase", "a phase detector coupled to the reference phase accumulator, the phase detector containing circuitry to compute a difference between the reference phase and a variable phase", "a digitally-controlled oscillator (DCO) coupled to the phase detector, wherein the performance of the DCO can be ascertained by a test circuit outside of the circuit observing an output of the phase detector, wherein the test circuit manipulates the observed output and generates a performance metric for the DCO based, at least in part, on the manipulation" arid "a variable phase accumulator coupled to the DCO and the phase detector, the variable phase accumulator containing circuitry to compute the variable phase". Applicants respectfully traverse Examiner's determination (pp. 11 of the office ac~on) that "Claim 41 is a system claim corresponding to method claim 1" and further determination that "Hence, the steps performed in method claim I would have necessitated the elements in system claim 41." Claim 41 is an apparatus claim that contains limitations obviously not present in method claim 1, including: "reference phase*

accumulator", "digitally controlled oscillator" and "variable phase accumulator". Applicants respectfully point out that, "all words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970). The above clearly shows that Examiner did not consider all of the limitations of Claim 41. Accordingly, the 35 U.S.C. 103(a) is improper and must be withdrawn. Further, even were the rejection to not be improper on its face, Claim 41 would be allowable for similar reasons as those set forth in the allowability of Claim 1. Accordingly, the 35 U.S.C. 103(a) rejection is improper and must be withdrawn".

The examiner respectfully agrees. However, a new ground of rejection has been issued in order to substantiate for this limitation.

Applicant further asserts that, *"Skierszkan discloses an acquisition PLL that has a low pass filter with a relatively high cut-off frequency. The acquisition PLL tracks all changes in the input signal, including error components." In actuality, the "acquisition PLL" is a separate PLL and adding a new PLL to the DPLL in Girardeau would not work since having two PLL's would bring issues of their differing performances, such as jitter or drift. The two PLL's would have separate oscillators and each oscillator is independent. Since the topic of Girardeau's invention is testing, now Girardeau's tests would need to be duplicated without solving the fundamental issue of setting the PLL into different bandwidth. Accordingly, Examiner's combination of Girardeau, Yamaguchi and Skierszkan and corresponding rejection of Claim 24 is improper and must be withdrawn".*

The examiner respectfully disagrees. One skilled in the art would know that the loop bandwidth must be set prior to turning the PLL on.

Applicant further asserts that, *"Combining Kim into Girardeau does not make sense because the objective of the DPLL in Girardeau is not test or even built-in self-test (BIST) but the main or mission mode of its operation, which includes agility and being robust over the changing environment. Girardeau teaches an apparatus and method for determining a feedback divider ratio in a digital phase locked loop (DPLL) by monitoring the drift in the feedback signal. The drift could be caused by using an unknown frequency of fixed frequency system clock 22. (col. 2, lines 28-39). Hence monitoring the frequency drift of the external clock is not related to testing, so there is no motivation to incorporate Kim. Furthermore, the test or BIST would imply reporting back the results outside of the circuit. No such mechanism is reported in Girardeau simply because he does not teach the test or BIST. Accordingly, the 35 U.S.C. 103(a) rejection is improper and must be withdrawn".*

The examiner respectfully disagrees. One skilled in the art would have founded obvious to incorporate the features in Kim into the system of Girardeau in order to come up with applicant's claimed invention.

Applicant further asserts that, *"Wong's system is engineered in such as way as to minimize the data rate accessible through the I/O controller. Hence, the phase detector 10 output is not accessible nor is the PEP 12 output - making them available (despite various technical difficulties) would not provide any substantial benefits. For the above reasons, Wong does not teach or suggest, "a control signal input coupled to the*

processor, wherein the control signal input can enable an observation and manipulation of the digital signals." The interface in Wong is asynchronous and there is simply no motivation to re-engineer the entire architecture, which in itself is non-obvious to one of average skill in the art at the time of the invention, to allow synchronous signal controls of sufficient speed, as suggested by Examiner. Accordingly, the 35 U.S.C. 103(a) rejection is improper and must be withdrawn".

The examiner respectfully disagrees. The reference of Wong does suggest the teachings of the claimed invention as described in figs 1-2 and table 2)

Applicant further asserts that, *"the phase detector 10 output contains information of the phase error, which is the phase difference between the Din and P_CLK inputs to the phase detector. FAP 26 register, on the other hand, contains "the frequency difference between Din and the local clock generated by the local crystal" (col. 4, lines 60-62) - this is definitely not the phase error. Hence, the tester 4 is not coupled to the phase detector. Accordingly, the 35 U.S.C. 103(a) rejection is improper and must be withdrawn".*

The examiner respectfully disagrees. One skilled in the art would know that there is a relationship between the frequency and the phase. However, taking the contrary, in figure 2, the reference of Wong does teach the IO controller coupled to the Phase access port.

Applicant further asserts that, *"the cited text by Examiner does not show any teaching from Wong "wherein the circuit permits the testing of the RF circuit in wafer". The circuit in Wong does not have the inventive features of the present invention to be*

testable on wafer. The link controller makes it simply unfeasible to reliably connect all the I/O signals between the circuit on wafer and the external tester".

The examiner respectfully disagrees. One skilled in the art would know that ICs are made out of wafers.

Applicant finally asserts that, *"Examiner's statement, however, does not establish "manipulating the signal outside of the RF circuit", as positively recited and required by Claim 1, OR "... wherein the performance of the DCO can be ascertained by a test circuit outside of the circuit observing an output of the phase detector, wherein the test circuit manipulates the observed output and generates a performance metric for the DCO based, at least in part, on the manipulation", as required by Claim 41. Wong only shows that some unrelated signal is being manipulated by an external tester. Previously, Examiner equated the "signal" to the phase detector output 30/32 or 104 in Girardeau. Now, Examiner alleges that Wong teaches that the 1-bit signal 104 could be accessed by the external digital tester 4 in a similar way as the FAP 26 could be read. This combination will not work. The 1-bit signal 104 contains its information not only in the binary value (i.e., early/late) but also in its time position (e.g., see Figure 2: in relation with 106 and 108). Transporting the 104 signal across the asynchronous and lower-speed IO controller 22 and Link 6 in Wong would destroy its time position information, thus making the circuit inoperable. Hence, it is not possible to combine Wong with Girardeau in the manner suggested by Examiner in order to obviate the above claim limitations. Accordingly, no prima facie case of obviousness has been established for Claims 1 and 41. The 35 U.S.C. 103(a) rejection of Claims 1 and 41 is*

improper and must be withdrawn".

The examiner respectfully disagrees. In col. 4, lines 62-65 the reference of Wong does teach that the digital tester averages "manipulates" several readings of FAP, and based on the result calculates the expected output frequency. Furthermore, in col. 1, line 38 - col. 2, line 3, the reference of Wong does teach the digital tester computes the PLL dynamic performance. And this is what applicant's claimed invention is trying to do.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in Graham v. John Deere Co., 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

1. Claims (1, 3, 5-8, 11, 13-14, 24-29, 31, 41-43) are rejected under 35 U.S.C. 103(a) as being unpatentable over Staszewski et al. (hereinafter Staszewski) (US Publication 2002/0191727 A1) in view of Wong et al. (hereinafter Wong) (US Patent 5,295,079)

Re claim 1, Staszewski discloses a method for testing a radio frequency (RF) circuit comprising: observing a signal from the RF circuit, wherein the signal is a digital signal from within a processing portion of the RF circuit. (See fig. 4A: "PHE")

But the reference of Staszewski fails to explicitly teach that wherein the signal has a high degree of correlation with an RF output of the RF circuit.

However, one skilled in the art would know that if the loop filter is designed in such as way (adjusting filter's parameters) so that the frequency of the error signal is within the cutoff frequency of the loop filter, then a high degree of correlation can be achieved between the error signal and the output signal.

Therefore, it would have been obvious to one of ordinary skills in the art to incorporate this feature into the system of Staszewski, in the manner as claimed, for the benefit of achieving synchronization.

The reference of Staszewski discloses the limitations as claimed, except he fails to explicitly teach that wherein the observing occurs outside of the RF circuit; manipulating the signal outside of the RF circuit; and producing a metric for the test outside of the RF circuit based on results from the manipulating.

However, Wong does. The reference of Wong does teach "to enhance accuracy, the digital tester 4 averages several readings of FAP 26. Based on the average reading

of FAP 26, the digital tester 4 calculates the expected output frequency (fm) of the PFC 16". (See col. 4, lines 59-65) By averaging several readings of FAP, the tester is somehow manipulating data from the PLL.

Furthermore, the reference of Wong also teaches "these digital signals are accessible through several on-chip (PLL) read/write ports allowing an external intelligent digital circuit (the tester) to compute the PLL dynamic performance" (See col. 1, lines 45-48), "providing a digital testing approach to measure RXC jitter" (See col. 4, lines 50-52), and this is done "by calculating the difference between the measured, PAP 28 readings and the predicted PAP 28 contents", and these readings are illustrated in an oscilloscope. (See col. 5, lines 6-16 & fig. 4)

And finally, Wong also teaches a table which lists the various tests necessary to ensure the proper functioning of a typical PLL circuit. (See col. 6, lines 29-36 & Table 2) Please note that in table 2, a spectrum analyzer is used in order to test FCO clock spectral purity). One skilled in the art would know that the spectrum analyzer (signal analyzer) is capable of observing, manipulating, and generating performance metrics.

Taking the combined teachings of Staszewski and Wong as a whole, it would have been obvious to one of ordinary skills in the art to have incorporated this feature into the system of Staszewski, in the manner as claimed and as taught by Wong, for the benefit of optimizing the performance of the PLL.

Re claim 3, the combination of Staszewski and Wong further discloses that wherein the signal is a phase error signal. (In Staszewski, see fig. 4A: "PHE")

Re claim 5, the combination of Staszewski and Wong fails to explicitly teach that that wherein a transfer function between the signal and the RF output phase is flat within a frequency band of interest.

However, one skilled in the art would know that if the loop filter is designed in such as way (adjusting filter's parameters) so that the frequency of the error signal is within the cutoff frequency of the loop filter, then a high degree of correlation can be achieved between the error signal and the output signal. Furthermore, when a high degree of correlation is achieved the transfer function will be flat within a specific frequency range.)

Therefore, it would have been obvious to one of ordinary skills in the art to incorporate this feature into the system of Staszewski, as modified by Wong, in the manner as claimed, for the benefit of achieving synchronization.

Re claim 6, the combination of Staszewski and Wong further discloses that wherein the RF circuit is an all-digital circuit, and wherein the signal is an output of a component in an all-digital phase-locked loop in the RF circuit. (In Staszewski, see fig. 4A)

Re claim 7, the combination of Staszewski and Wong further discloses that wherein the signal is an output of a phase detector. (In Staszewski, see fig. 4A: "PHE" & 68)

Re claim 8, the combination of Staszewski and Wong further discloses that wherein the signal has been filtered. (In Wong, see fig. 2: 14)

Re claim 11, the combination of Staszewski and Wong further discloses that wherein a loop filter coupled to an output of a phase detector performs the filtering, and wherein the signal is an output of the loop filter. (In Wong, see fig. 2: 14)

Re claim 13, the combination of Staszewski and Wong further discloses that wherein the frequency of the signal is several orders of magnitude less than the frequency of the RF output. (One skilled in the art would know that the frequency of the error signal, outputted from the phase comparator, is less than the RF frequency.)

Re claim 14, the combination of Staszewski and Wong fails to disclose that wherein the test is for phase error trajectory and the signal is the output of a phase detector, and wherein the manipulation comprises measuring a change in the signal.

However, the reference of Wong does teach measuring a change phase error outputted from the phase detector. (See fig. 2: 26 & 28 & figs. 3A, 4A, 4B, 4C)

Therefore, it would have been obvious to one of ordinary skills in the art to incorporate this feature into the system of Staszewski, as modified by Wong, in the manner as claimed, for the benefit of achieving synchronization.

Re claim 24, the combination of Staszewski and Wong further discloses that wherein the RF circuit contains an all-digital phase-locked loop. (In Staszewski, see fig. 4A)

But the combination of Girardeau and Yamaguchi fails to explicitly teach that the method further comprises prior to the observing, setting the all-digital phase-locked loop to a certain bandwidth.

However, the reference of Wong does teach a loop configuration circuit which in response to the digital tester programs and via the LCP configures the loop type of the Device under test "DUT". (See col. 3, lines 19-26 & table 1)

Therefore, it would have been obvious to one of ordinary skills in the art to incorporate this feature into the system of Staszewski, as modified by Wong, in the manner as claimed, for the benefit of achieving synchronization.

Re claim 25, the combination of Staszewski and Wong fails to explicitly teach that wherein the test is for estimating phase noise power and the signal is an output of a phase detector, and wherein the manipulating comprises calculating a mean square error of the signal.

However, the reference of Wong does suggest calculating RXC jitter by phase meter. (See col. 4, line 41 - col. 5, line 16) Furthermore, one skilled in the art would know that the mean square error of the signal can be computed once the phase error is determined.

Therefore, it would have been obvious to one of ordinary skills in the art to incorporate this feature into the system of Staszewski, as modified by Wong, in the manner as claimed, for the benefit of achieving synchronization.

Re claim 26, the combination of Staszewski and Wong fails to explicitly teach that wherein the setting, observing, and manipulating is repeated for several different all-digital phase-locked loop bandwidths, and wherein the producing comprises subtracting the calculated mean square errors for the several different all-digital phase-lock loop bandwidths.

However, the reference of Wong does suggest selecting loop configuration based on selected application, and minimizing the phase error signal in order to achieve frequency/phase lock. (See col. 3, lines 19-26) Furthermore, one skilled in the art would know that the loop bandwidth varies depending if the PLL is in either acquisition or tracking mode.

Therefore, it would have been obvious to one of ordinary skills in the art to incorporate this feature into the system of Staszewski, as modified by Wong, in the manner as claimed, for the benefit of achieving synchronization.

Re claim 27, the combination of Staszewski and Wong further discloses that wherein the RF circuit is an all-digital frequency synthesizer. (In Staszewski, see fig. 4A)

Re claim 28, the combination of Staszewski and Wong further discloses that wherein the RF circuit is an all-digital transmitter. (In Staszewski, see paragraph 59)

Re claim 29, the combination of Staszewski and Wong further discloses that wherein the transmitter is used in a wireless communications network. (In Staszewski, see paragraph 59)

Re claim 31, the combination of Girardeau and Yamaguchi further discloses that wherein the testing comprises a functional test or a compliance test of the RF circuit. (In Wong, see col. 1, line 38 – col. 2, line 3)

Re claim 41, Staszewski discloses a circuit comprising: a reference phase accumulator coupled to a signal input, the reference phase accumulator containing circuitry to compute a reference phase (See fig. 4A: 62 & paragraph 44); a phase detector coupled to the reference phase accumulator, the phase detector containing circuitry to compute a difference between the reference phase and a variable phase (See fig. 4A: 68 & paragraph 44); a digitally-controlled oscillator (DCO) coupled to the phase detector (See fig. 4A: 74 & paragraph 44), a variable phase accumulator coupled to the DCO and the phase detector, the variable phase accumulator containing circuitry to compute the variable phase. (See fig. 4A: 66 & paragraph 46)

But the reference of Staszewski fails to teach that wherein the performance of the DCO can be ascertained by a test circuit outside of the circuit observing an output of

the phase detector, wherein the test circuit manipulates the observed output and generates a performance metric for the DCO based, at least in part, on the manipulation.

However, Wong does. The reference of Wong does teach "to enhance accuracy, the digital tester 4 averages several readings of FAP 26. Based on the average reading of FAP 26, the digital tester 4 calculates the expected output frequency (fm) of the PFC 16". (See col. 4, lines 59-65) By averaging several readings of FAP, the tester is somehow manipulating data from the PLL.

Furthermore, the reference of Wong also teaches "these digital signals are accessible through several on-chip (PLL) read/write ports allowing an external intelligent digital circuit (the tester) to compute the PLL dynamic performance" (See col. 1, lines 45-48), "providing a digital testing approach to measure RXC jitter" (See col. 4, lines 50-52), and this is done "by calculating the difference between the measured, PAP 28 readings and the predicted PAP 28 contents", and these readings are illustrated in an oscilloscope. (See col. 5, lines 6-16 & fig. 4)

And finally, Wong also teaches a table which lists the various tests necessary to ensure the proper functioning of a typical PLL circuit. (See col. 6, lines 29-36 & Table 2) Please note that in table 2, a spectrum analyzer is used in order to test FCO clock spectral purity). One skilled in the art would know that the spectrum analyzer (signal analyzer) is capable of observing, manipulating, and generating performance metrics.

Taking the combined teachings of Staszewski and Wong as a whole, it would have been obvious to one of ordinary skills in the art to have incorporated this feature

into the system of Staszewski, in the manner as claimed and as taught by Wong, for the benefit of optimizing the performance of the PLL.

Re claim 42, the combination of Staszewski and Wong further disclose a time-to-digital converter (TDC) coupled to the DCO and the phase detector, the TDC containing circuitry to compute a time difference between a reference clock and a variable clock. (In Staszewski, see fig. 6 & paragraph 51)

Re claim 43, the combination of Staszewski and Wong fails to explicitly teach a loop filter coupled to the phase detector and the DCO, the loop filter to provide a desired amount of attenuation to the computed difference between the reference phase and the variable phase.

However, the reference of Staszewski does teach a loop gain coupled to the phase detector and the DCO. (See fig. 4A: 70) One skilled in the art would know that the loop gain is a function of the loop filter and other parameters within the PLL.

Therefore, it would have been obvious to one of ordinary skills in the art to incorporate this feature into the system of Staszewski, as modified by Wong, in the manner as claimed, for the benefit of achieving synchronization.

2. Claims (15-17, 19-21) are rejected under 35 U.S.C. 103(a) as being unpatentable over Staszewski et al. (hereinafter Staszewski) (US Publication 2002/0191727 A1) and Wong et al. (hereinafter Wong) (US Patent 5,295,079), as applied to claim 1 above, and further in view of Girardeau, Jr. (hereinafter Girardeau) (US Patent 5,486,792)

Re claim 15, the combination of Staszewski and Wong fails to explicitly teach that wherein the phase error trajectory is good when the change in the signal is less than a specified threshold.

However, Girardeau does. (See fig. 2: error signal & col. 5, lines 37-39) Girardeau discloses a digital phase lock loop "DPLL" wherein an error signal is generated based on a comparison between a reference signal and a feedback signal. The error signal is further compared with a threshold in order to determine if a coarse or fine adjustment is needed.

Taking the combined teachings of Staszewski, Wong, and Girardeau as a whole, it would have been obvious to one of ordinary skills in the art to have incorporated this feature into the system of Staszewski, as modified by Wong, in the manner as claimed and as taught by Girardeau, for the benefit of optimizing the performance of the PLL.

Re claim 16, the combination of Staszewski, Wong, and Girardeau further discloses that wherein the measuring the change in the signal comprises measuring a peak, a variance, or a rate of change in the signal. (In Girardeau, see fig. 2: error signal.

And see col. 5, lines 37-39)

Re claim 17, the combination of Staszewski, Wong, and Girardeau further discloses that wherein the test is for frequency lock and the signal is the output of a phase detector (In Girardeau, see col. 2, lines 30-37 & col. 4, lines 65-67), and wherein the manipulation comprises comparing a value of the signal over several samples. (In Girardeau, see fig. 2 & col. 5, lines 37-40. The error signal is being compared with the threshold. Furthermore, during tracking mode the PLL tries to keep the phase locked.)

Re claim 19, the combination of Staszewski, Wong, and Girardeau further discloses that wherein the samples are taken at different times. (In Girardeau, see fig. 2 & col. 5, lines 37-40. The error signal is being compared with the threshold. Furthermore, during tracking mode the PLL tries to keep the phase locked.)

Re claim 20, the combination of Staszewski, Wong, and Girardeau further discloses that wherein the test is for frequency deviation and the signal is an output of an integral accumulator of a loop filter (In Girardeau, see col. 5, lines 19-21), and wherein the manipulation comprises comparing the signal with a specified range. (In Girardeau, see col. 2, lines 30-36. The error signal is being compared with the threshold.)

Re claim 21, the combination of Staszewski, Wong, and Girardeau further discloses that wherein the frequency deviation is within acceptable limits when the signal is within the specified range. (In Girardeau, see col. 2, lines 30-36)

Re claim 22, the combination of Staszewski, Wong, and Girardeau further discloses that wherein the manipulation further comprises comparing several samples of the signal. (In Girardeau, see fig. 2 & col. 5, lines 37-40. The error signal is being compared with the threshold.)

Claim 45 is rejected under 35 U.S.C. 103(a) as being unpatentable over Girardeau, Jr. (hereinafter Girardeau) (US Patent 5,486,792) and Yamaguchi et al. (hereinafter Yamaguchi) (US Patent 6,687,629 B1), as applied to claims 1 & 41 above, and further in view of Ko. (US Patent 5,982,832)

Re claim 45, the combination of Staszewski and Wong fails to disclose that wherein the loop filter is comprised of a plurality of filters, and wherein the filters are arranged in a parallel fashion.

However, Ko does. (See fig. 4 & col. 4, lines 18-25) Ko discloses a plurality of filters arranged in a parallel fashion.

Therefore, taking the combined teachings of Staszewski, Wong and Ko as a whole. It would have been obvious to one of ordinary skills in the art to have incorporated this feature into the system of Staszewski, as modified by Wong, in the

manner as claimed and as taught by Ko, for the benefit of achieving phase compensation.

Claim 46 is rejected under 35 U.S.C. 103(a) as being unpatentable over Girardeau, Jr. (hereinafter Girardeau) (US Patent 5,486,792) and Yamaguchi et al. (hereinafter Yamaguchi) (US Patent 6,687,629 B1), as applied to claims 1 & 41 above, and further in view of Cucchietti et al. (hereinafter Cucchietti) (US Patent 4,819,080)

Re claim 46, the combination of Staszewski and Wong fails to disclose that wherein the loop filter is comprised of a plurality of filters, and wherein the filters are arranged in a cascaded fashion.

However, Cucchietti does. (See fig. 4: "BP" & col. 2, lines 45-52) Cucchietti discloses two cascaded filters located at the output of a phase detector.

Therefore, taking the combined teachings of Staszewski, Wong, and Cucchietti as a whole, it would have been obvious to one of ordinary skills in the art to have incorporated this feature into the system of Staszewski, as modified by Wong, in the manner as claimed and as taught by Cucchietti, for the benefit of achieving passing the desired frequencies and eliminating the non-desired frequencies.

1. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Staszewski et al. (hereinafter Staszewski) (US Publication 2002/0191727 A1) and Wong et al. (hereinafter Wong) (US Patent 5,295,079), as applied to claim 1 above, and further in view of Kim et al (hereinafter Kim) (US Patent 6,885,700 B1).

Re claim 2, the combination of Staszewski and Wong fails to specifically disclose that wherein the testing is performed using built-in self-test (BIST) techniques.

However, Kim does. (See abstract & col. 1, lines 13-40) Kim discloses a charge-based frequency technique that performs structural and defect-oriented testing and uses existing blocks to save die area.

Taking the combined teachings of Staszewski, Wong, and Kim as a whole, it would have been obvious to one of ordinary skill in the art to have modified the system of Staszewski, as modified by Wong, in the manner as claimed and as taught by Kim, for the benefit of providing proper stimulus for the loop filter located inside the PLL.

Claims (10 & 44) are rejected under 35 U.S.C. 103(a) as being unpatentable over Staszewski et al. (hereinafter Staszewski) (US Publication 2002/0191727 A1) and Wong et al. (hereinafter Wong) (US Patent 5,295,079), as applied to claim 1 above, and further in view of Mathe et al (hereinafter Mathe) (US Patent 5,825,253).

Re claim 10, the combination of Staszewski and Wong fails to specifically disclose that wherein the all-digital phase-lock loop is operating in a type-I mode, and the signal is an output of an infinite impulse response filter coupled to the output of a loop filter.

However, Mathe does. (See col. 5, lines 32-37) Mathe discloses a phase lock loop that contains a loop filter which can be implemented as a digital filter such as an infinite impulse response (IIR) filter.

Therefore, taking the combined teachings of Staszewski, Wong, and Mathe as a whole, it would have been obvious to one of ordinary skill in the art to have modified the system Staszewski, as modified by Wong, in the manner as claimed and as taught by Mathe, for the benefit of providing synthesis of both zeros and poles in the filter. (See col. 9, lines 55-56)

Re claim 44, the motivation for combining these two references has already been established in claim 10 above, therefore, the combination of Staszewski, Wong, and Mathe further discloses that wherein the loop filter is of a type selected from a group consisting of a finite impulse response filter, an infinite impulse response filter or combination thereof. (In Mathe, see col. 5, lines 32-37 & col. 9, lines 55-56)

Claims (9, 12, 30 & 47) are rejected under 35 U.S.C. 103(a) as being unpatentable over Staszewski et al. (hereinafter Staszewski) (US Publication 2002/0191727 A1) and Wong et al. (hereinafter Wong) (US Patent 5,295,079), as applied to claims 1 & 41 above, and further in view of Staszewski et al. (hereinafter Staszewski I) (US Publication 2002/0094052 A1)

Re claim 9, the combination of Staszewski and Wong further disclose, that the signal is an output of an integral accumulator of a loop filter. (See col. 3, lines 14-15)

But the combination of Staszewski and Wong fails to teach that wherein the all-digital phase-lock loop is operating in a type-II mode.

However, Staszewski I does. (See paragraph 2)

Taking the combined teachings of Staszewski, Wong, and Staszewski I as a whole, it would have been obvious to one of ordinary skill in the art to have modified the system Staszewski, as modified by Wong, in the manner as claimed, and as taught by Staszewski I, for the benefit of optimizing the PLL.

Re claim 12, the combination of Staszewski, Wong, and Staszewski I further disclose that wherein the signal is an output of a gain normalization block. (In Staszewski I, see fig. 5: "DCO Gain Normalization")

Re claim 30, the combination of Staszewski, Wong, and Staszewski I further discloses that wherein the wireless communications network is Bluetooth compliant. (In Staszewski I, see paragraph 32)

Re claim 47, Staszewski, Wong, and Staszewski I a gain normalization unit coupled to the phase detector and the DCO, the gain normalization unit to normalize the difference between the reference phase and the variable phase with respect to a gain in the DCO. (In Staszewski I, see fig. 5: "DCO Gain Normalization")

Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Staszewski et al. (hereinafter Staszewski) (US Publication 2002/0191727 A1) and Wong et al. (hereinafter Wong) (US Patent 5,295,079), as applied to claim 1 above, and further in view of Gustafson et al (hereinafter Gustafson) (US Patent 4,086,539).

Re claim 18, the combination of Staszewski and Wong fails to specifically disclose that wherein if a variance in the magnitude is less than a specified threshold, then the frequency has been locked.

However, Gustafson does. (See abstract & col. 1, lines 37-40) Gustafson discloses that phase lock loops produce favorable results in terms of phase-error variance in high frequency system and below threshold.

Taking the combined teachings of Staszewski, Wong, and Gustafson as a whole, it would have been obvious to one of ordinary skill in the art to have modified the system Staszewski, as modified by Wong, in the manner as claimed, and as taught by Gustafson, for the benefit of locking the frequency.

3. Claims (32-40) are rejected under 35 U.S.C. 103(a) as being unpatentable over Wong et al. (hereinafter Wong) (US Patent 5,295,079)

Re claim 32, Wong discloses a circuit comprising: a processor coupled to a radio frequency (RF) circuit. (See fig. 2)

But the reference of Wong fails to explicitly teach that the processor containing circuitry to manipulate digital signals from the RF circuit to provide a performance metric

for the RF circuit; and a control signal input coupled to the processor, wherein the control signal input can enable an observation and manipulation of the digital signals.

However, the reference of Wong does suggest that the teachings of digital tester (an intelligent digital controller) coupled to an input "keyboard" (See fig. 1: the input of element 4 & col. 1, lines 56-61), that performs tests, extract, and interpret data from the device under test (DUT). Furthermore, table 2 shows several of how to test some PLL dynamic performance parameters. (See fig. 2: 4 & col. 1, lines 45-48, 56-61, col. 2, lines 36-40, col. 4, lines 6-15)

Therefore, it would have been obvious to one of ordinary skills in the art to have incorporated this feature into the system of Wong, in the manner as claimed, for the benefit of testing some PLL dynamic performance parameters. (See col. 6, lines 29-31)

Re claim 33, the reference of Wong fails to disclose a latch coupled to the processor, the latch to store the performance metric provided by the processor.

However, the reference of Wong does suggest the teaching of a digital tester, which may be a hand-held microprocessor-based controller with a keyboard and a multi-digit display that can be used for network servicing or for low-cost lab-quality engineering setups. (See col. 4, lines 13-16) Furthermore, one skilled in the art would know that latches may be used as storage elements, from which flip-flops are usually constructed. And registers, which are used extensively in the design of digital systems for storing data, consists of a set of flip-flops.

Therefore, it would have been obvious to one of ordinary skills in the art to have incorporated this feature into the system of Wong, in the manner as claimed, for the benefit of testing some PLL dynamic performance parameters. (See col. 6, lines 29-31)

Re claim 34, the combination of Wong further discloses that wherein the RF circuit is integrated onto a first integrated circuit, wherein the processor is integrated onto a second integrated circuit. (In Wong, see fig. 2)

Re claim 35, the reference of Wong fails to explicitly teach that wherein the first and the second integrated circuit are the same integrated circuit.

However, the reference of Wong does suggest the teaching of a IO controller integrated within the same integrated circuit as the RF circuit. (See fig. 2: 22 & 25)

Therefore, it would have been obvious to one of ordinary skills in the art to have incorporated this feature into the system of Wong, in the manner as claimed, for the benefit of minimizing the time delay.

Re claim 36, the combination of Wong further discloses that wherein the RF circuit contains an all-digital phase-locked loop, and wherein the processor is coupled to an output of a phase detector. (In Wong, see fig. 2)

Re claim 37, the combination of Wong further discloses that wherein the RF circuit contains an all-digital phase-locked loop, and wherein the processor is coupled to

a filtered output of a phase detector. (In Wong, see fig. 2: 24 & col. 3, lines 19-22, 50-56)

Re claim 38, the combination of Wong further discloses that wherein the RF circuit contains an all-digital phase-locked loop, and wherein the processor is coupled to an output of a phase detector and a filtered output of a phase detector. (In Wong, see fig. 2 & col. 3, lines 50-55)

Re claim 39, the combination of Wong further discloses that wherein the circuit permits the testing of the RF circuit in wafer, in packaged integrated circuit, in factory, and in field. (In Wong, see col. 1, lines 38-41, 48-51 & col. 4, lines 16-27)

Re claim 40, the combination of Wong further discloses that wherein the circuit permits the testing of the RF circuit, and wherein the testing is of a type selected from a group consisting of a phase trajectory error, a frequency lock, a frequency deviation, a phase noise power, or combinations thereof. (In Wong, see fig. 2, 4b & 4c & col. 4, line 34 – col. 6, line 35 & table 2)

2. Claims (48-50, 52-54) are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al (hereinafter Kim) (US Patent 6,885,700 B1) in view of Ortiz Perez et al. (hereinafter Perez) (US Patent 5,966,428)

Re claim 48, Kim discloses a method for operating a cellular phone, comprising:

performing built-in self-test (BIST) on a parameter associated with the cellular phone. (See col. 6, lines 9-49 "PLL")

But the reference of Kim fails to teach reporting to a cellular service provider through a wireless medium when the BIST reports the parameter to be degraded beyond a limit.

However, Perez does. (See abstract & col. 5, line 26 – col. 6, line 15) Perez discloses a self-diagnostic system for checking all functions of a cellular-transceiver, and reporting the results to an off-site monitoring center by means of the cellular network.

Taking the combined teachings of Kim and Perez as a whole, it would have been obvious to one of ordinary skills in the art to incorporate this feature into the system of Kim, in the manner as claimed and as taught by Perez, for the benefit of reporting the results to an off-site monitoring center.

Re claim 49, the combination of Kim and Perez fails to explicitly teach that wherein the performing step is done on power-up of the cellular phone.

However, the reference of Perez does teach that the system for checking all the functions of the cellular is a self-diagnostic system. (See abstract) Furthermore, it also teaches that it is an auto-diagnostic system. One skilled in the art would know that auto-diagnostic system operate at power-up of the cellular phone to assure that the tranceiver is working properly.

Therefore, it would have been obvious to one of ordinary skills in the art to incorporate this feature into the system of Kim, as modified by Perez, in the manner as claimed, for the benefit of checking if the cellular phone is working properly.

Re claim 50, the combination of Kim and Perez further discloses that wherein the parameter is an RF system parameter. (In Kim, see col. 6, lines 9-49 "PLL")

Re claim 52, the combination of Kim and Perez fails to explicitly teach that a step of notifying a user of the cellular phone that the parameter is degraded beyond a limit.

However, the reference of Perez does teach a self-diagnostic system for checking all functions of a cellular-transceiver, and reporting the results to an off-site monitoring center by means of the cellular network in order to check if the tranceiver is working properly.

Therefore, it would have been obvious to one of ordinary skills in the art to incorporate this feature into the system of Kim, as modified by Perez, in the manner as claimed, for the benefit of checking if the cellular phone is working properly.

Re claim 53, the combination of Kim and Perez further discloses that wherein the notifying step is done wirelessly. (In Perez, see abstract “cellular network”)

Re claim 54, the combination of Kim and Perez fails to explicitly teach that wherein the notifying step is done through a service bill.

However, the reference of Perez does teach notifying the results to an off-site monitoring center by means of the cellular network. One skilled in the art would know that service bill can also be broadcast wirelessly.

Therefore, it would have been obvious to one of ordinary skills in the art to incorporate this feature into the system of Kim, as modified by Perez, in the manner as claimed, for the benefit of optimizing the communication system.

3. Claim 51 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al (hereinafter Kim) (US Patent 6,885,700 B1) and Ortiz Perez et al. (hereinafter Perez) (US Patent 5,966,428), as applied to claim 48 above, and further in view of Reddy et al. (hereinafter Reddy) (US Patent 6,636,979 B1)

Re claim 51, the combination of Kim and Perez fails to explicitly teach that wherein the RF system parameter is a distortion in a phase error trajectory.

However, Reddy does. (See col. 5, lines 58-65) Reddy discloses a phase error measurement circuit used to measure the phase error between two clocks. The circuit can be used as part of a built-in self test (BIST) function to estimate phase error in a PLL.

Taking the combined teachings of Kim, Perez, and Reddy as a whole, it would have been obvious to one of ordinary skills in the art to incorporate this feature into the system of Kim, as modified by Perez, in the manner as claimed and as taught by Reddy, for the benefit of detecting the phase error.

4. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Staszewski et al. (hereinafter Staszewski) in view of Yamaguchi et al. (hereinafter Yamaguchi) (US Patent 6,687,629 B1)

Re claim 1, Staszewski discloses a method for testing a radio frequency (RF) circuit comprising: observing a signal from the RF circuit, wherein the signal is a digital signal from within a processing portion of the RF circuit. (See fig. 4A: "PHE")

But the reference of Staszewski fails to explicitly teach that wherein the signal has a high degree of correlation with an RF output of the RF circuit.

However, one skilled in the art would know that if the loop filter is designed in such as way (adjusting filter's parameters) so that the frequency of the error signal is within the cutoff frequency of the loop filter, then a high degree of correlation can be achieved between the error signal and the output signal.

Therefore, it would have been obvious to one of ordinary skills in the art to incorporate this feature into the system of Staszewski, in the manner as claimed, for the benefit of achieving synchronization.

The reference of Staszewski discloses the limitations as claimed, except he fails to explicitly teach that wherein the observing occurs outside of the RF circuit; manipulating the signal outside of the RF circuit; and producing a metric for the test outside of the RF circuit based on results from the manipulating.

However, Yamaguchi does. (See fig. 29) Yamaguchi discloses a spectrum analyzer connected to the output of a phase detector, and located outside an RF circuit and a PLL. One skilled in the art would know that the spectrum analyzer (signal

analyzer) is capable of observing, manipulating, and generating performance metrics. Furthermore, the concept of measuring and observing the phase detector output outside of a PLL is taught by the reference of Yamaguchi. (See fig. 29) Subsequently, one skilled in the art would have founded obvious to connect a spectrum analyzer to a PLL in order to measure and observe the output of the phase detector, as taught by Yamaguchi.

Taking the combined teachings of Staszewski and Yamaguchi as a whole, it would have been obvious to one of ordinary skills in the art to have incorporated this feature into the system of Staszewski, in the manner as claimed and as taught by Yamaguchi, for the benefit of optimizing the performance of the PLL.

Contact

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LEON FLORES whose telephone number is (571)270-1201. The examiner can normally be reached on Mon-Fri 7-5pm Alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Payne can be reached on 571-272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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